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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,687	01/14/2002	Jingo Nakanishi	57454-315	9036

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,687	NAKANISHI, JINGO	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,19 and 20* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's response to the restriction requirement filed on 2/13/03 has been received and entered in the case. The following is a detailed Office Action of the elected species II, i.e., claims 1-4 and 19-20.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses language which can be implied, i.e., "according to the invention". Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: the summary of invention section and its header are missing.

Appropriate correction is required.

Claim Objections

4. Claims 19-20 are objected to because of the following informalities:

In claim 19, line 9, "a control signal" should be changed to -- said control signal--.

In claim 20, line 11, "a control signal" should be changed to -- said control signal--,

line 27, "a capacitor" should be changed to -- said capacitor --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,385,265, issued to Duffy et al.

As per claim 1, Duffy discloses a clock synchronizer (Fig. 3) generating a second clock signal VCO_CLK synchronized with a first clock signal CLOCK, comprising:

a phase difference detection circuit (comparator 102) detecting a phase difference between said first and second clock signals (CLOCK, VCO_CLK), and setting a first control signal (PUMPUP, PUMPDN) to be at an activated level (the voltage level of the PUMPUP and/or PUMPDN signal) for a time period corresponding to the phase difference;

a loop filter (110) connected to a predetermined node FILTU;

a current-supply circuit (charge pump 106 and common mode control 104) supplying current to said loop filter (110) in response to the first control signal (PUMPUP, PUMPDN) from said phase difference detection circuit (102); and

a clock generating circuit (voltage controlled oscillator 108) generating said second clock signal (VCO_CLK) in accordance with a potential (the potential at node FILTU) of said predetermined node FILTU;

said current-supply circuit (106 and 104, Fig. 4 is the details of circuit 106) including

a variable current source (transistor 166a) whose output current can be controlled (by the signal CM_PBIAS),

a first switching circuit (transistors 170a) passing output current of said variable current source (transistor 166a) through said loop filter (110) in response to that said first signal (PUMPUP, PUMPDN) is set to be at the activated level, and

a first control circuit (common mode control 104) controlling said variable current source (transistor 166a) such that predetermined constant current flows from said variable current

source to said loop filter (110), based on the potential (CM_PBIAS) of said predetermined node FILTU.

As per claim 2, Duffy further discloses

said variable current source (transistor 166a) includes a first transistor (transistor 166a) of a first conductivity type (P-type) whose input electrode receives a first control potential (CM_PBIAS),

said first switching circuit (transistor 170a) connects said first transistor 166a between a line of a first power-supply potential (the supply voltage VCC) and said loop filter (110) in response to that said first control signal (PUMPUP, PUMPDN) is set to be at the activated level, and

said first control circuit (common mode control circuit 104) controls said first control potential (CM_PBIAS) such that predetermined constant current flows through said first transistor (transistor 166a) connected between the line of said first power-supply potential (VCC) and said loop filter (110), based on the potential of said predetermined node FILTU.

As per claim 19, Duffy et al. discloses a clock synchronizer (Fig. 3) generating a second clock signal VCO_CLK synchronized with a first clock signal CLOCK, comprising:

a phase difference detection circuit (102) detecting a phase difference between said first and second clock signals (CLOCK, VCO_CLK) and setting a control signal (PUMPUP, PUMPDN) to be at an activated level for a time period corresponding to the phase difference;

a loop filter (110) connected to a predetermined node FILTU;

a current-supply circuit (circuits 106 and 104) supplying current to said loop filter (110) in response to said control signal (PUMPUP, PUMPDN) from said phase difference detection circuit (102); and

a clock generating circuit (108) generating said second clock signal (VCO_CLK) in accordance with a control potential (CM_PBIAS, as shown in Fig. 6, FILU controls the signal CM_PBIAS);

said current-supply circuit (circuits 104 and 106) including

a transistor (166a, Fig. 4) whose input electrode receives said control potential (CM_PBIAS),

a switching circuit (transistor 170a) connecting said transistor 166a between a line of a power-supply potential (power supply VCC) and said loop filter (110), in response to that said control signal (PUMPUP, PUMPDN) is set to be at an activated level, and

a control circuit (common mode control 104) controlling said control potential (CM_PBIAS) such that predetermined constant current flows through said transistor (166a) connected between the line of said power-supply potential (VCC) and said loop filter (110), based on a potential of said predetermined node FILTU.

As per claim 20, Duffy discloses a clock synchronizer (Fig. 3) generating a second clock signal (VCO_CLK) synchronized with a first clock signal (CLK), comprising:

a phase difference detection circuit (102) detecting a phase difference between said first and second clock signals (CLK, VCO_CLK), and setting a control signal (PUMPUP, PUMPDN) to be at an activated level for a time period corresponding to the phase difference;

a loop filter (110) including a resistance element (column 3, lines 12-15) and a capacitor (also see column 3, lines 12-15) connected between a predetermined node FILTU and a line of a reference potential GND;

a current-supply circuit (106 and 104) supplying current to said loop filter (110) in response to said control signal (PUMPUP, PUMPDN) from said phase difference detection circuit (102); and

a clock generating circuit (109) generating said second clock signal (VCO_CLK) in accordance with a potential of said predetermined node FILTU;

said current-supply circuit (circuits 104 and 106) including

a transistor (166a, Fig. 4) whose input electrode receives a control potential (CM_PBIAS),

a switching circuit (transistor 170a) connecting said transistor (166a) between a line of a power-supply potential (the power supply VCC) and said loop filter (110), in response to that said control signal (PUMPUP, PUMPDN) is set to be at an activated level, and

a control circuit (104) controlling said control potential (CM_PBIAS) such that predetermined constant current flows through said transistor (166a) connected between the line of said power-supply potential VCC and said loop filter (110), based on a potential (VC') of a node between said resistance element and a capacitor (this limitation is met because Duffy's loop filter 110 comprises resistors and capacitors, column 3, lines 12-15, clearly there are connections between resistors and capacitors, a potential of one of these nodes reads on the recited potential VC').

Allowable Subject Matter

6. Claim 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-4 are allowable because the prior art of record fails to disclose or suggest a clock synchronizer which includes a first control circuit wherein the first control circuit having a second, third transistors and first resistance element connected as recited in claim 3.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,781,048, 5,334,953, 5,687,201, 5,475,326 disclose various PLL circuits which have control circuits fed back from the loop filters to the charge pump circuits which also read on some of the claims.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
March 7, 2003